Cond. A7

proves difficult to remove in high aspect ratio storage containers (0.5μ inside diameter by 1.5μ high).

Referring now to FIG. 6, both oxides 21 and 31, which have different etch rates, are now exposed. At this point, an oxide etch is performed such that oxide 31 is completely removed from inside container 51 while a portion of oxide 21 remains at the base of container 51 and thereby providing an insulating layer between the underlying topography and subsequent layers. [A] An etch rate ratio of 2:1 or greater between (a ratio of 4:1 is preferred) oxide 31 and oxide [22] 21 provides sufficient process margin to ensure all of high etch rate oxide 31 inside container 51 is removed during the single etch step, while a portion of oxide [22] 21 remains to provide adequate insulation from subsequently formed layers.

Referring now to FIG. 7, when using this structure to form a capacitor storage node plate container 51, [and] the remaining portion of oxide 21 is coated with a capacitor cell dielectric 71. [And, finally] Finally a second conformal poly layer 72 is placed [to] onto blanket cell dielectric 71 and serves as a common capacitor cell plate to the entire array of containers 51. From this point on, the wafer is completed using conventional fabrication process steps.

IN THE CLAIMS:

Please cancel claims 1 through 60.